Amendments to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. (Withdrawn) A method of fabricating a dual damascene interconnection with a metal-insulator-metal capacitor, the method comprising:

forming a via-level intermetal dielectric on a substrate where first and second lower metal interconnections are formed;

forming a via hole for connecting a lower electrode of a metal-insulator-metal capacitor and the first lower metal interconnection by patterning the via-level intermetal dielectric;

sequentially forming a metal layer for a capacitor lower electrode, a capacitor dielectric layer, and a metal layer for a capacitor upper electrode on the entire surface of the substrate;

forming the metal-insulator-metal capacitor, which includes a lower electrode, a dielectric layer, and an upper electrode, by patterning the metal layer for the lower electrode, the capacitor dielectric layer, and the metal layer for the upper electrode, which are disposed over the via hole;

forming a trench-level intermetal dielectric on the via-level intermetal dielectric including the metal-insulator-metal capacitor;

simultaneously forming a groove for a dual damascene interconnection, exposing the second lower metal interconnection, and a trench exposing the upper electrode by etching the via-level intermetal dielectric and the trench-level intermetal dielectric; and

forming a dual damascene interconnection connected to the second lower metal interconnection and an upper metal interconnection connected to the upper electrode by filling the groove for the dual damascene interconnection and the trench with a metal.

2. (Withdrawn) The method of claim 1, wherein the formation of the first lower

metal interconnection and the second metal interconnection comprises:

forming an insulating layer on the substrate; and

forming the first lower metal interconnection and the second lower metal interconnection by filling the insulating layer with a metal using a damascene process.

3. (Withdrawn) The method of claim 1, wherein the via hole is formed in a hole shape.

4. (Withdrawn) The method of claim 1, wherein the via hole is formed in a line shape.

5. (Withdrawn) The method of claim 1, further comprising:

forming an etch stop layer between the first and second lower metal interconnections and the via-level intermetal dielectric; and

forming another etch stop layer between the via-level intermetal dielectric and the trench-level intermetal dielectric.

6. (Withdrawn) The method of claim 1, further comprising forming the metal-insulator-metal capacitor using one masking process and then reducing the area of the upper electrode by etching edges of the upper electrode.

7. (Withdrawn) The method of claim 1, wherein the lower electrode directly contacts the first lower metal interconnection by the via hole.

8. (Withdrawn) The method of claim 1, after forming the via hole, further comprising forming a via for connecting the lower electrode and the first lower metal interconnection by filling the via hole with a conductive material and then planarizing the filled

conductive material.

9. (Withdrawn) The method of claim 1, wherein the formation of the groove for the dual damascene interconnection includes forming the via hole and the line trench using a via-first dual damascene process.

10. (Withdrawn) The method of claim 9, wherein, while the line trench is being formed, the trench exposing the upper electrode is formed.

11. (Withdrawn) The method of claim 1, wherein the formation of the groove for the dual damascene interconnection includes forming a via hole and a line trench using a line trench-first dual damascene process.

12. (Withdrawn) The method of claim 1, wherein the dual damascene interconnection is formed of at least one material selected from the group consisting of copper, gold, silver, tungsten, and any alloy thereof.

13. (Withdrawn) The method of claim 1, wherein, while the via hole for connecting the lower electrode of the metal-insulator-metal capacitor and the first lower metal interconnection is being formed, an alignment key for aligning the metal-insulator-metal capacitor is formed by patterning the via-level intermetal dielectric.

14. (Withdrawn) The method of claim 13, wherein the formation of the metal-insulator-metal capacitor includes leaving the metal layer for the lower electrode, the capacitor dielectric layer, and the metal layer for the upper electrode on the inner walls of the alignment key by performing an anisotropic etchback process.

15. (Withdrawn) The method of claim 13, wherein, while the dual damascene interconnection and the upper metal interconnection are being formed, a dummy interconnection is formed by filling a stepped region of the alignment key.

16. (Currently Amended) A dual damascene interconnection structure with a metal-insulator-metal capacitor, the structure comprising:

a via-level intermetal dielectric and a trench-level intermetal dielectric which are sequentially stacked on a substrate;

a dual damascene interconnection formed in the via-level intermetal dielectric and the trench-level intermetal dielectric including a line trench extending through the trench-level intermetal dielectric to the via-level intermetal dielectric; and

a metal-insulator-metal capacitor formed between the via-level intermetal dielectric and the trench-level intermetal dielectric to include a lower electrode, a dielectric layer, and an upper electrode.

17. (Original) The structure of claim 16, further comprising:

a first lower metal interconnection and a second lower metal interconnection, which are formed between the substrate and the via-level intermetal dielectric;

a via which is included in the via-level intermetal dielectric to connect the lower electrode and the first lower metal interconnection; and

an upper metal interconnection formed on and connected to the upper electrode, wherein the dual damascene interconnection is connected to the second lower metal interconnection.

18. (Original) The structure of claim 17, wherein the first lower metal interconnection and the second lower metal interconnection are damascene interconnections buried in an insulating layer formed on the substrate.

19. (Original) The structure of claim 17, wherein the via is filled in a hole-type opening.

20. (Original) The structure of claim 17, wherein the via is filled in a line-type opening.

21. (Original) The structure of claim 16, wherein the lower electrode, the dielectric layer, and the upper electrode are patterned to have the same area.

22. (Original) The structure of claim 16, wherein the upper electrode is patterned to have a smaller area than that of each of the lower electrode and the capacitor dielectric layer.

23. (Original) The structure of claim 17, wherein the via is integrally formed with the lower electrode.

24. (Original) The structure of claim 16, further comprising an alignment key formed in the via-level intermetal dielectric so as to have the step difference to align the metal-insulator-metal capacitor.

25. (Original) The structure of claim 24, further comprising the metal layer for the lower electrode, the dielectric layer, and the metal layer for the upper electrode on the inner walls of the alignment key.

26. (Original) The structure of claim 24, further comprising a dummy interconnection in a stepped region of the alignment key.

27. (Original) The structure of claim 16, wherein the dual damascene interconnection is formed of at least one material selected from the group consisting of copper, gold, silver, tungsten, and any alloy thereof.

28. (Original) The structure of claim 17, wherein the via and the dual damascene interconnection are formed of different materials.

29. (Original) The structure of claim 16, further comprising:

a first lower metal interconnection and a second lower metal interconnection formed between the substrate and the via-level intermetal dielectric; and

an upper metal interconnection formed on and connected to the upper electrode, wherein the lower electrode is directly connected to the first lower metal interconnection, and the dual damascene interconnection is connected to the second metal interconnection.

30. (Currently Amended) The structure of claim 16, wherein the dual damascene interconnection further includes a via hole formed in the via-level intermetal dielectric ~~and a line trench formed in the trench-level intermetal dielectric~~.

31. (Previously Presented) The structure of claim 30, further comprising:

an upper metal interconnection positioned in a trench, wherein the trench is formed in the trench-level intermetal dielectric to expose the upper electrode.

32. (Currently Amended) The structure of claim 17, wherein the dual damascene interconnection further includes a via hole formed in the via-level intermetal dielectric ~~and a line trench formed in the trench-level intermetal dielectric~~.

33. (Previously Presented) The structure of claim 32, wherein the upper metal interconnection is positioned in a trench, wherein the trench is formed in the trench-level intermetal dielectric to expose the upper electrode.

34. (New) A dual damascene interconnection structure with a metal-insulator-metal capacitor, the structure comprising:

a via-level intermetal dielectric and a trench-level intermetal dielectric which are sequentially stacked on a substrate;

a dual damascene interconnection formed in the via-level intermetal dielectric and the trench-level intermetal dielectric;

a metal-insulator-metal capacitor formed between the via-level intermetal dielectric and the trench-level intermetal dielectric to include a lower electrode, a dielectric layer, and an upper electrode; and

an alignment key formed in the via-level intermetal dielectric so as to have the step difference to align the metal-insulator-metal capacitor.

35. (New) The structure of claim 34, further comprising the metal layer for the lower electrode, the dielectric layer, and the metal layer for the upper electrode on the inner walls of the alignment key.

36. (New) The structure of claim 34, further comprising a dummy interconnection in a stepped region of the alignment key.